- isolation means (4) between the input/output module (2) and the encryption module (3), for making the sensitive information stored in the encryption module (3) inaccessible to the host system (HS) and for ensuring the parallelism of the operations performed by the input/output module (2) and the encryption module (3).

16. An encryption circuit according to claim 15, characterized in that the isolation means (4) of the circuit (1) comprises a double-port memory (4).

17. An encryption circuit according to claim 15 wherein this isolation means (4) comprises a double port memory coupled between the input/output module (2) and the encryption module (3), the dual-port memory (4) being coupled to a first bus and adapted to simultaneously handle the exchange of data, commands and statuses between the input/output and encryption modules (2 and 3), and isolation between the two modules (2 and 3).

18. An encryption circuit is set forth in claim 15, characterized in that the encryption module (3) comprises:

- a first encryption sub-module (3_1), dedicated to the processing of symmetric encryption algorithms, and being coupled with the first bus of the dual port memory (4);

- a second encryption sub-module (3_2), dedicated to the processing of asymmetric encryption algorithms (40) and being coupled with the first bus of the dual-port memory (4) and including a separate internal second bus isolated from the first bus of the dual-port memory (4); and

- a CMOS memory (11) coupled with the dual-port memory (4) via the first bus of the dual-port memory containing the encryption keys.

19. An encryption circuit as set forth in claim 16, characterized in that the encryption modules (3) comprises:

- a first encryption sub-module (3_1), dedicated to the processing of symmetric encryption algorithms, and being coupled with the first bus of the dual port memory (4);

- a second encryption sub-module (3_2), dedicated to the processing of asymmetric encryption algorithms (40) and being coupled with the first bus of the dual-port memory (4) and including a separate internal second bus isolated from the first bus of the dual-port memory (4); and

- a CMOS memory (11) coupled with the dual-port memory (4) via the first bus of the dual-port memory containing the encryption keys.

20. An encryption circuit as set forth in claim 17, characterized in that the encryption module (3) comprises:

- a first encryption sub-module (3_1), dedicated to the processing of symmetric encryption algorithms, and being coupled with the first bus of the dual port memory (4);

- a second encryption sub-module (3_2), dedicated to the processing of asymmetric encryption algorithms (40) and being coupled with the first bus of the dual-port memory (4) and including a separate internal second bus isolated from the first bus of the dual-port memory (4); and

- a CMOS memory (11) coupled with the dual-port memory (4) via the first bus of the dual-port memory containing the encryption keys.

21. an encryption circuit according to claim 18, characterized in that the first encryption sub-module (3_1) comprises an encryption component (9) coupled with the dual-port memory (4) via the first bus of the memory (4), comprising various encryption automata, respectively dedicated to the processing of symmetric encryption algorithms, and in that the second encryption sub-module (3_2) comprises at least two encryption processors (10_1 and 10_2), respectively dedicated tot he processing of asymmetric encryption algorithms, coupled with the encryption module (9) via the internal second bus of the second sub-module (3_2) and a bus isolator (14) for isolating the second bus from the first bus of the dual port memory.

22. An encryption circuit according to claim 21, characterized in that the encryption processors (10_1 and 10_2) of the encryption module (30 are of the CIP type.

23. An encryption circuit according to claim 21, characterized in that one (10_1) of the two encryption processors (10_1 and 10_2) is of the CIP type, and in that the other (10_2) of the two encryption processors is of the ACE type.

24. An encryption circuit according to claim 21, characterized in that one of the two encryption processor (10_2) is of the ACE type comprising a field programmable gate array (FPGA).

25. An encryption circuit according to claim 24, characterized in that the encryption component (9) is of the SCE type.

26. An encryption circuit according to claim 25, characterized in that the encryption component (9) comprises a field programmable array (FPGA).

27. An encryption circuit according to claim 26, characterized in that the second encryption sub-module (3_2) comprises a flash memory PROM (12) and an SRAM memory (13) coupled with the second internal bus of the sub-module (3_2).

28. An encryption circuit according to claim 21, further comprising a CMOS memory (11) containing security keys and security mechanisms (15) adapted to trigger a reset mechanism of the CMOS memory (11) in case of an alarm.

29. an encryption circuit according to claim 15 characterized in that the input/output module (2) comprises:

- a microcontroller (6) having an input/output processor (6_1) and a PCI interface (6_2) integrating DMA channels responsible for executing the data transfers between the host system (HS) and the circuit (1);

- a flash memory (7) containing the code of the input/output processor (6_1) and a PCI interface (6_2) integrating DMA channels responsible for executing the data transfers between the host system (HS) and the circuit (1);

- a flash memory (7) containing the code of the input/output processor (6_1); and

- an SRAM memory (8) that receives a copy of the contents of the flash memory (7) upon startup of the input/output processor (6_1).